Design of a Restartable Crystal Controlled Clock for Use in a Globally Asynchronous, Locally Synchronous Design Methodology

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ECE595 Masters Project Report

Abstract:

This paper presents the design of a restartable crystal controlled clock. The clock generator is a critical component in a newly proposed blended design methodology which combines clockless and clocked subsystems and is a special case of a Globally Asynchronous Locally Synchronous (GALS) design strategy. The clock generator has been successfully implemented in the TSMC 0.25μm NWELL process, occupies an area of 0.016mm^2 (700 NAND gate equivalents), dissipates 20 mW of power, and operates at frequencies up to 200 MHz. The delay in starting the clock is 6 nsec +/- 45 ps.

Keywords: Globally Asynchronous Locally Synchronous (GALS), clock generator, synchronizer failure, restartable crystal controlled clock.

1.0 Introduction

Currently, Globally Asynchronous Locally Synchronous (GALS) [1] systems suffer from either poor control of the local clock period or the potential for synchronizer failure [2]. Synchronizer failures occur when setup and hold time constraints are violated in a system consisting of flip-flops or registers. If these requirements are not met, there is the possibility that the flip-flop can be held up in a logic level which cannot be resolved to known logic levels of either a '0' or '1'. This is a metastable state [3] and theoretically the flip-flop can spend an infinite amount of time in this state.

In general, due to asymmetries in signal levels in the implementation of logic gates and due to inherent noise in the circuit, the flip-flop eventually exits the metastable state. This delay in exiting the metastable region is sometimes, however, sufficient for a system to crash. The possibility of flip-flops entering a metastable state is high in an asynchronous system whose inputs do not depend upon the clock edge as they can change at any instant of time, violating setup and hold time requirements.

There are three common ways to deal with synchronizer failure [3]. The first way is to reduce the clock rate which in turn gives sufficient time for the flip-flop to settle. This is not an efficient technique because reducing clock speeds reduces the performance of the system. The second approach often used is to place two synchronizers in between the asynchronous input and the rest of the synchronous circuit. This technique decreases the probability of both synchronizers going into metastability simultaneously, thereby reducing the probability of synchronizer failure. This method involves complex design, and there is still the possibility of the flip-flops entering the metastable state.

The third approach is to follow a timing strategy that is independent of the speed of the individual circuits. This third strategy deals with the generation of a clock locally and forces the processing units to communicate with each other using delay-insensitive signaling conventions [4]. The proposed clock generator is designed for use in this type of methodology that successfully *eliminates* the possibility of synchronizer failures. Thus, the clock generator is a critical component in a blended methodology which combines clockless and clocked subsystems [2] and is a special case of a Globally Asynchronous Locally Synchronous (GALS) design strategy.

In Section 2 the blended approach is presented which describes the control wrapper and the clock generator that is to be embedded along with the data processing subsystems. Section 3 explains design of a clock generator (and its subcircuits) which can be started at any instant of time. The simulation results obtained for the clock generator are presented under Section 4 followed by discussion of the physical layout and future work.

2.0 Blended Methodology

Figure 1 has been adopted from [2] in which the data processing subsystem is embedded in a control wrapper along with the clock generator.

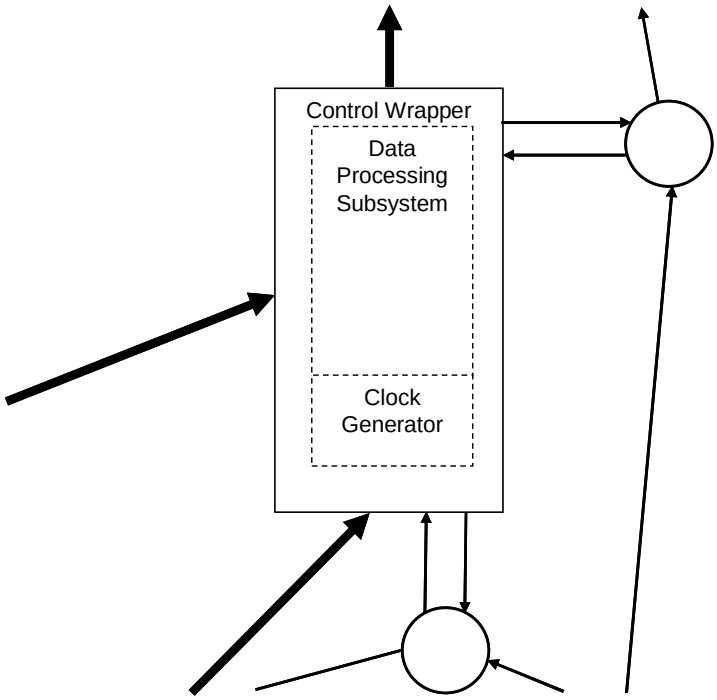

Figure 1. Data processing subsystem with a control wrapper and the clock generator

The clock generator serves as a local clock to it. The heavy solid lines indicate data paths between different data processing subsystems and lighter lines indicate sequencing paths between control elements indicated by circles.

2.1 Control Wrapper

The purpose of the control wrapper [2] is to initiate the local clock of the data processing subsystem and to signal an acknowledgement indicating that the action is completed. An example of the control wrapper where and is shown in Figure 2. The control wrapper is designed by using macromodular control elements and in general the details of the

control wrapper depend on the nature of the sequencing network in which it has been embedded.

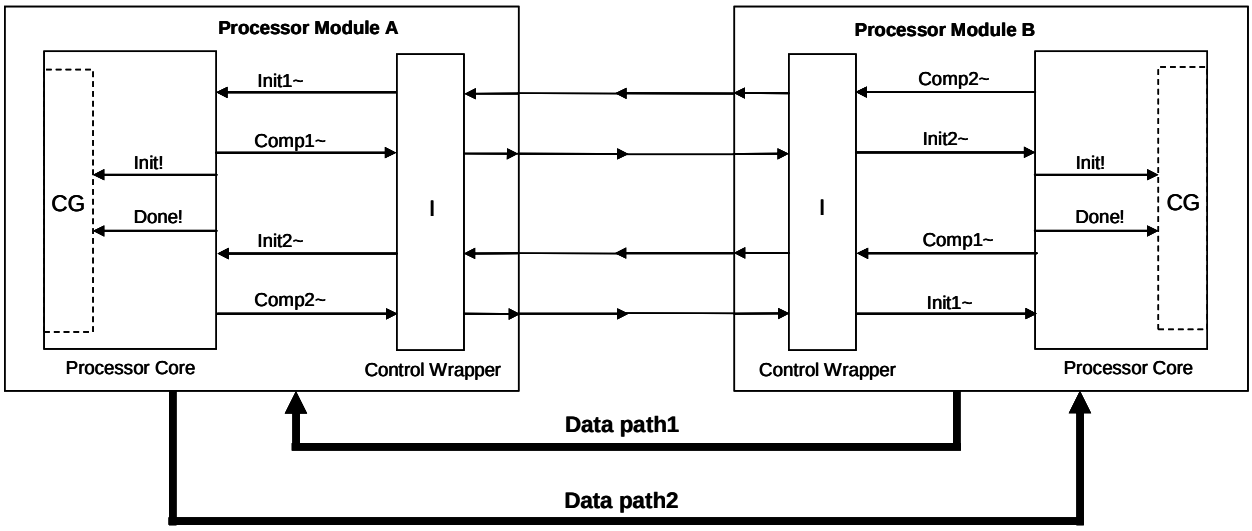

Figure2: Blending the clock generator into data processing subsystem

2.2 Clock Generator

The clock generator is based on a stable crystal oscillator, but functions more like a delay based clock generator. Unlike a crystal oscillator, the clock generator can be started or stopped [5] at any instant of time by taking on a phase reference determined by the starting instant. The block diagram of the clock generator is shown in Figure 3. The '*!*' suffix on signal names indicates pulse signaling which means that the signal has to return to its previous level. Signal names with no suffix indicate level signaling is used.

The operation of the clock generator is based on the simple trigonometric identity [5] given by

$$\sin(\omega t) * \cos(\omega u) - \cos(\omega t) * \sin(\omega u) = \sin(\omega(t-u)) \qquad (1)$$

where 'ω' is the angular frequency in rad/sec, 't' is time in sec and '*u*' is the delay introduced with respect to the start of the crystal oscillator *i.e.* the assertion of one of the '*Init!*' signals.

The act of "starting" the clock is accomplished when either one of the '*Init!*' signals is asserted. This sets the output of one of the SR latches which initially are both reset. Setting one of the latches causes the '*RUN*' signal go high which in turn serves as the hold input to the sample and hold (S/H) circuits. The high level on the hold input of S/H circuits forces them into the hold mode.

The assertion of '*Done!*' resets both SR latches causing the '*RUN*' signal to return low. This will place the sample and hold (S/H) circuits into sampling mode in which the input is freely passed to the output. During the sampling phase, both multipliers yield to the same output which is $\sin(\omega t) \times \cos(\omega t)$. The multiplier outputs are applied as inputs to the comparator and the output of the comparator is driven low because of zero differential voltage seen at its inputs, thus "stopping" the clock.

As illustrated in Figure 3, each multiplier has four inputs which are in quadrature with one another. These quadrature inputs are generated from a crystal oscillator which is present externally or by a quadrature voltage controlled oscillator (QVCO) embedded in a phase locked loop (PLL) used for frequency synthesis located on the integrated circuit.

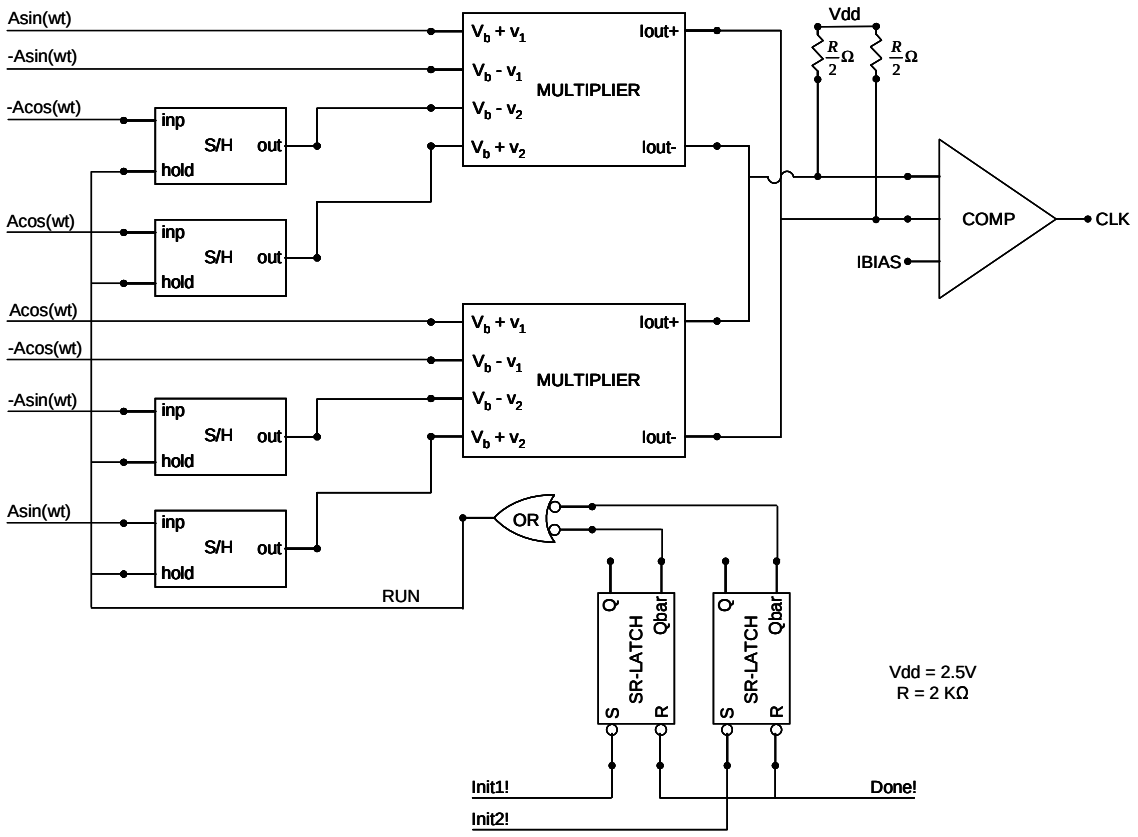

Figure 3. Clock generator

The top multiplier in Figure 3 produces an output which is $\sin(\omega t)\times\cos(\omega u)$ because the sine inputs to the multiplier are applied directly and the cosine inputs come from the outputs of the sample and hold circuits. The analog multiplier used is a fully differential (both input and output) structure so as to improve performance which will be explained in more detail in a later section of this report. The output of each of the multipliers is a differential current.

Similarly, the bottom multiplier produces an output equivalent to $\cos(\omega t)*\sin(\omega u)$. The outputs produced by the two multipliers when subtracted yield the identity given in equation (1). Since the output of the multipliers is a current and the comparator requires

a differential input voltage, two 1 KΩ pull-up resistors convert the pair of differential output currents to a differential voltage. The subtraction operation is then performed by a comparator which produces the required clock *i.e.* a square wave of frequency same as that of the crystal oscillator frequency.

3.0 Subsystem Design

Circuits needed in the design of the clock generator are an analog multiplier, a comparator, SR latches, and a quad sample and hold circuit. Design of the multiplier and the comparator circuits are critical in designing the clock generator and will be described in detail in the following sections.

3.1 Multiplier

The multiplier shown in Figure 4 has been adapted from [6]. It is a four quadrant analog multiplier based on the quarter square algebraic identity and is implemented by using six symmetrical structures called combiners. As shown in Figure 4, the multiplier is implemented using only NMOS transistors and resistors.

The reason for adopting this multiplier structure in designing the clock generator is its simple symmetrical structure thereby providing high bandwidth and large voltage swing (+/- 500 mV) which is especially important given the relatively low supply voltage of 2.5 Volts that we are currently using and the industry trend towards lower supply voltages in general. The resistors are realized by a high-resistance (1 kΩ per square) poly silicon layer available in the TSMC process.

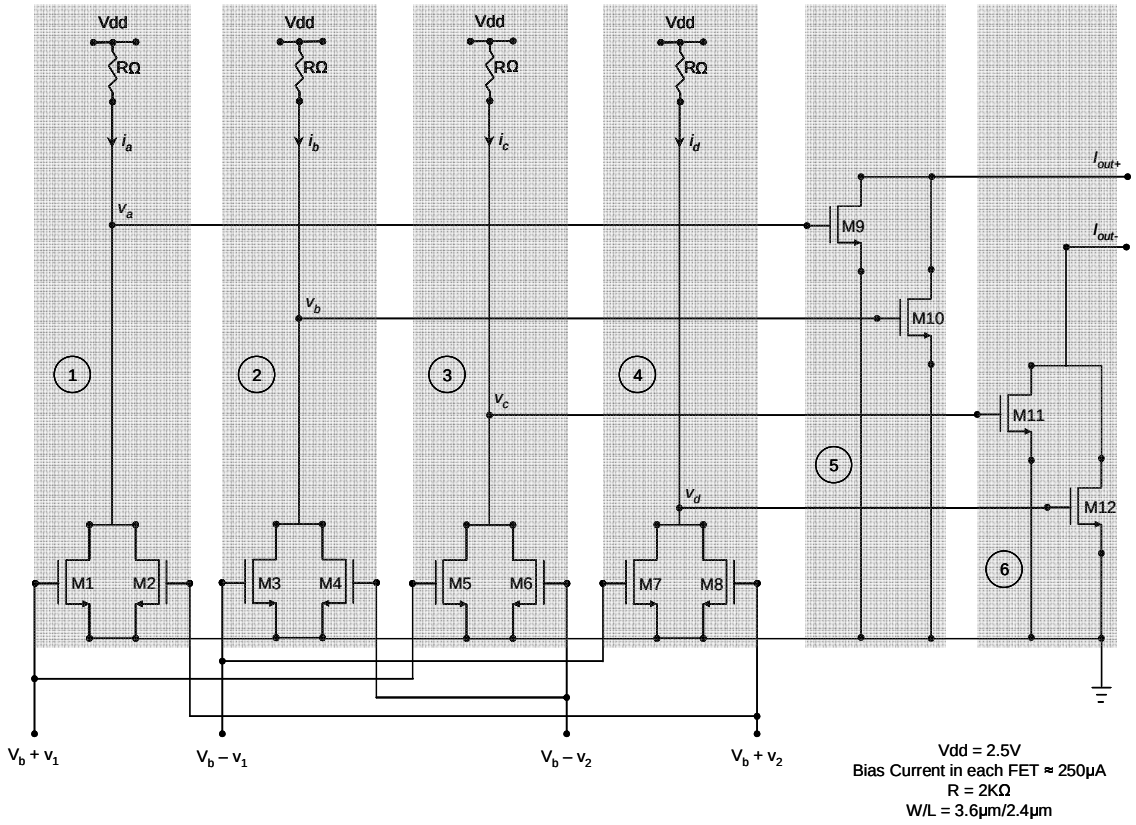

Figure 4. Multiplier circuit diagram

The NFETs in the analog multiplier have a shape factor of 3, and the length of each transistor is 2.4μm. The choice of dimensions was dictated by the need to ensure the FETs square-law I-V characteristic which is central to obtaining a good multiplier. Also, using large device sizes minimizes the effect of channel length modulation and also gives rise to more voltage head room at the output while operating at higher frequencies. Employing a channel area of $17\mu m^2$ ensures good matching. We estimate the 3σ mismatch in each of the various transistor pairs to be 7mV.

The large device sizes required to ensure the FET square-law characteristic and adequate matching also limit the maximum operating speed, the amount of area occupied by the

clock generator, and its ability to scale in size with reduction on process feature size. While possible to use somewhat smaller devices, the multiplier worked poorly when minimum length FETs (0.24μm) were used. When device lengths smaller that 1μm were tried, the square-law dependence of drain-to-source current on gate-to-source voltage is lacking, and the circuit fails to perform the multiply operation correctly.

All of the transistors in the analog multiplier are operated in saturation, and the current in each combiner can be represented by the square law identity of a MOS transistor given by

$$I_{DS} = \frac{1}{2n} K_{pn} S_n (V_{GS} - V_{Tn})^2 \qquad (2)$$

where I_{DS} is the drain to source current flowing in a transistor, V_{GS} is the gate to source voltage, V_{Tn} is the threshold voltage of the NFET, K_{pn} is the transconductance parameter of the NFET, n is the sub threshold slope factor, and S_n is the shape factor of each NFET.

Equation (2) represents the ideal square law characteristic of an NFET and does not consider non-linear effects such as channel length modulation, sub threshold leakage, and the body effect. These non ideal effects can be successfully reduced to a great percentage while designing the analog multiplier if device dimensions are kept large.

The output node voltage v_a of the first combiner shown in Figure 4 is given by

$$v_a = Vdd - i_a R \qquad (3a)$$

where R is the resistance, i_a is the sum of currents flowing in transistors M_1 and M_2 of the first combiner. The current flowing in each transistor is given by the expression in (2).

Substituting the input voltages $V_b + v_1$ and $V_b + v_2$ which are applied as gate voltages to the transistors M_1 and M_2 respectively, equation (3a) can be written as

$$v_a = Vdd - \frac{1}{2n} K_{pn} S_n R\left[(V_b + v_1 - V_{Tn})^2 + (V_b + v_2 - V_{Tn})^2\right] \qquad (3b)$$

Expanding the above equation and rearranging the terms we get a second order equation in terms of v_1 and v_2 which is shown below

$$v_a = -\frac{\beta_n R}{2n} v_1^{\,2} - \frac{\beta_n R}{2n} v_2^{\,2} - \frac{\beta_n R(V_b - V_{Tn})^2}{n} v_1 - \frac{\beta_n R(V_b - V_{Tn})^2}{n} v_2 + \left[Vdd - \frac{\beta_n R}{n}(V_b - V_{Tn})^2\right] \qquad (3c)$$

where $\beta_n = K_{pn} S_n$ called the gain factor of the transistor. Similarly, the output node voltages v_b through v_d for the combiners from 2 to 4 also have the same expression shown in equation (3c) except that the sign of the terms containing v_1 and v_2 change based on the phase of the signal that is applied to the corresponding combiner as shown in Figure 4.

The expressions for the output node currents I_{out+} and I_{out-} of the combiners 5 and 6 are given as

$$I_{out+} = \frac{\beta_n}{2n}\left[\left(v_a^{\,2} + v_b^{\,2}\right) - 2V_{Tn}\left(v_a + v_b\right) + 2V_{Tn}^{\,2}\right] \qquad (4a)$$

$$I_{out-} = \frac{\beta_n}{2n}\left[\left(v_c^{\,2} + v_d^{\,2}\right) - 2V_{Tn}\left(v_c + v_d\right) + 2V_{Tn}^{\,2}\right] \qquad (4b)$$

The output current of the analog multiplier I_{out} is thus obtained by subtracting equation (4b) from equation (4a) and after some algebraic manipulation we obtain the following expression

$$I_{out} = I_{out+} - I_{out-}$$
$$I_{out} = 32\left(\frac{\beta_n}{2n}\right)^3 R^2 (V_b - V_{Tn})^2 v_1 v_2 \qquad (5)$$

Equation (5) demonstrates that the multiplier circuit generates the product of the two applied signals v_1 and v_2. The output current produced is converted into a voltage by using a pull up resistor of 1KΩ and is applied as input to the comparator. In the proposed clock generator, the v_1 and v_2 signals are sinusoids generated by the crystal oscillator which is present externally or by a voltage controlled oscillator present in a phase locked loop.

Figure 5 shows a comparison between analytical (based on equation (5)) and simulated results of the output voltage waveforms generated by the multiplier. The plot labeled 'Differential Voltage' on its y-axis is the differential voltage that the comparator sees at its input. This waveform follows equation (1). If the input differential voltage is positive, the comparator output is pulled high and if it is negative the output is pulled low, thus generating a square wave which serves as clock to the data processing element. The input frequency applied to the multipliers is 100MHz. The phase difference between both waveforms is due to the delay inserted by SR latches, OR gate and S/H circuits before the multipliers, which is not considered in the analysis.

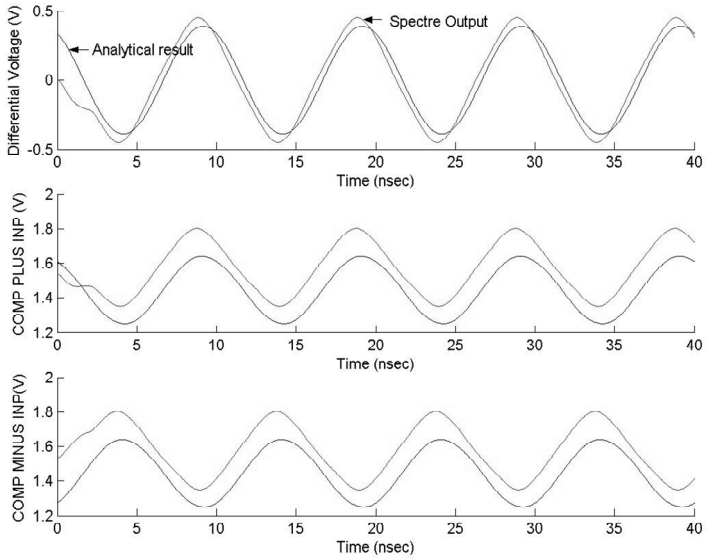

Figure 5. Comparison of analytical and simulated results

Figure 6 illustrates the simulated time domain output and spectrum of a single multiplier. The applied input frequency is 50 KHz. Since the multiplier is fully differential only odd harmonic distortion is present. The total harmonic distortion is 1 %.

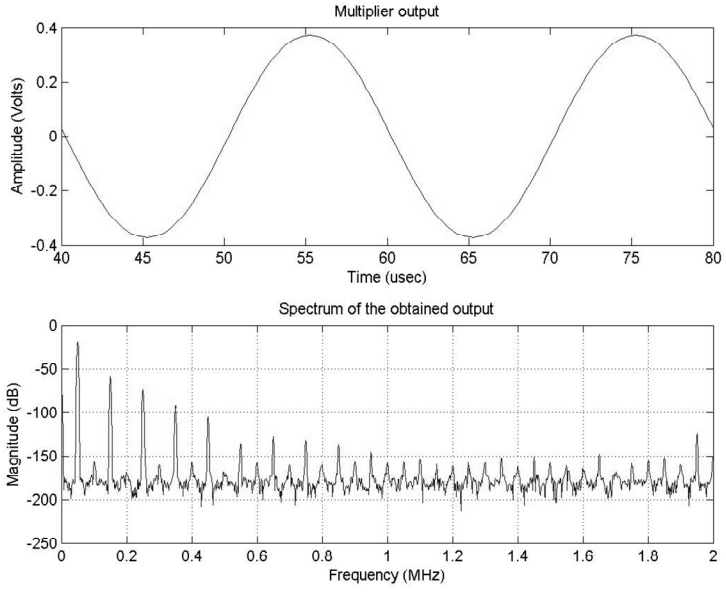

Figure 6. Spectrum of multiplier output

The linearity of the multiplier was also simulated by varying the v_2 input from – 500mV to +500mV while keeping the input v_1 constant. The linearity plots thus obtained are shown in Figure 7. The plots shown are for v_1 equal to -500mV and +500mV. The plots are comparable for the two polarities and the multiplier is reasonably linear over the range: +/- 400 mV. Lowering the amplitude of the v_1 input does not significantly improve the linearity.

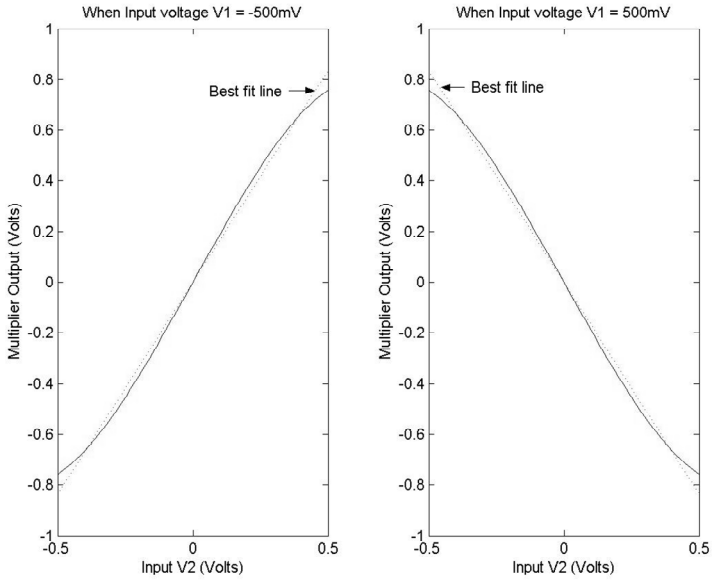

Figure 7. Linearity of the analog multiplier

The large signal bandwidth of a single multiplier simulated under a no-load condition is shown in Figure 8. The multiplier has a -3dB bandwidth of 600MHz under no-load. Even when inserted into the overall clock generator circuit the bandwidth remains approximately 600 MHz.

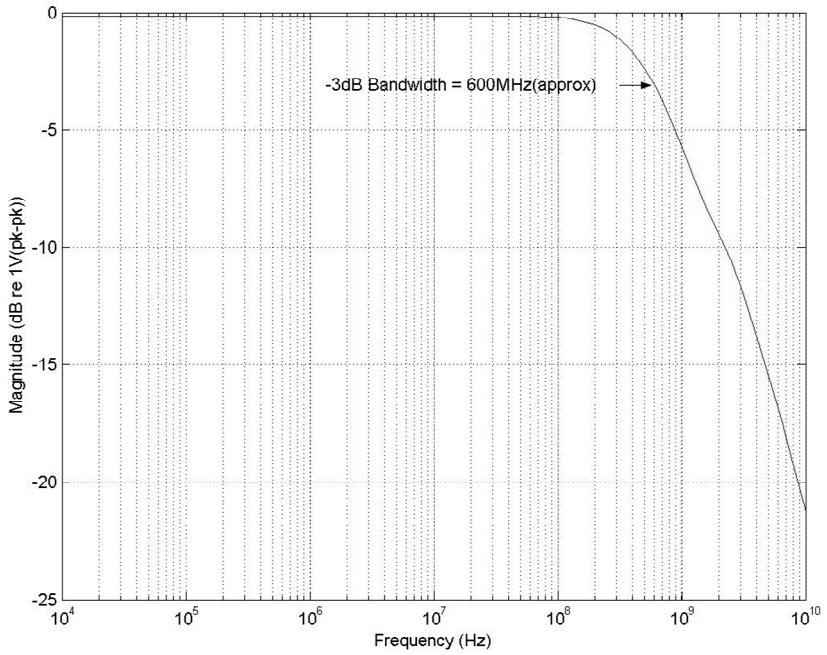

Figure 8: Frequency response of analog multiplier

3.2 Comparator

A differential input voltage comparator [7] shown in Figure 9 is used to convert the sinusoidal output from the multipliers into a square wave. The outputs from the multipliers are applied as inputs to the comparator as shown in Figure 3.

In Figure 9 the shape factors of the transistor pairs (M_1, M_2), (M_3, M_4), (M_5, M_6), (M_7, M_8), (M_9, M_{10}), (M_{11}, M_{12}) are equal and are indicated on top of each transistor. The multiplier outputs are applied to matched transistors M_3 and M_4 which form the input stage of the comparator. The transistors M_9 and M_{10} provide positive feedback in the input stage. This helps to improve the gain of first stage and thereby increases the resolution of the comparator.

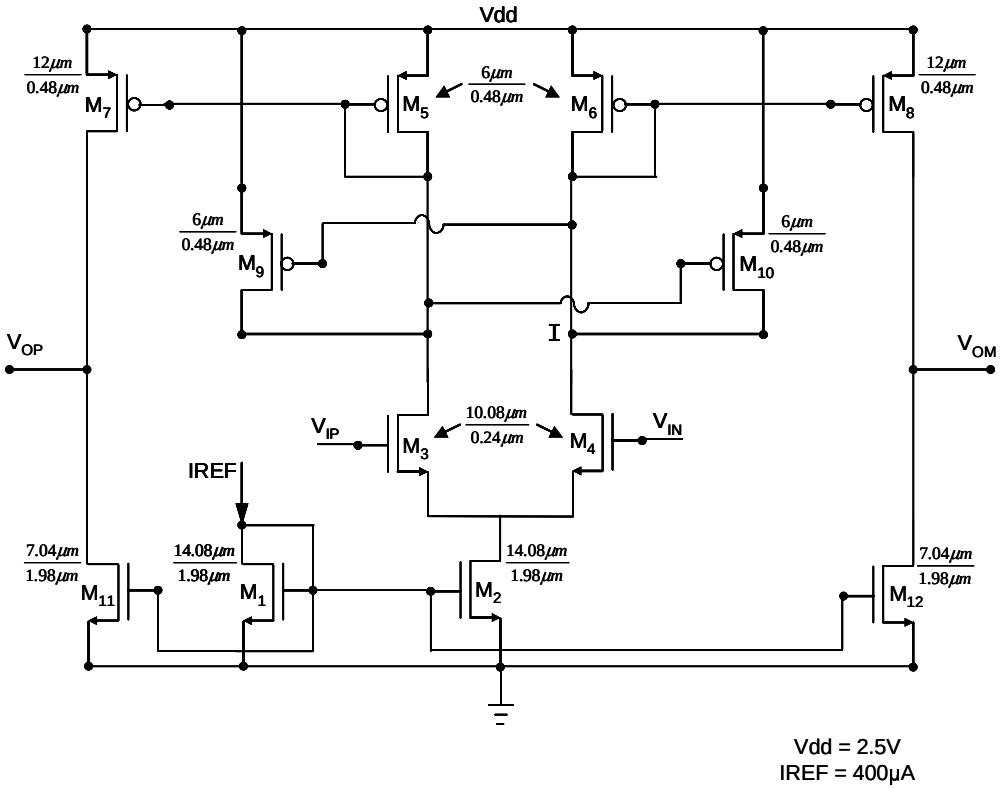

Figure 9: Comparator schematic

For analysis purposes, if the effect of feedback transistor M_{10} is neglected, the approximate voltage gain in the first stage of the comparator can be expressed as

$$A_{V1} \approx \frac{g_{m4}}{g_{m6}} \qquad (6)$$

where g_{m4} and g_{m6} are the transconductance parameters of M_4 and M_6 transistors respectively. The calculated value of g_{m4} is 1.6 milli-mhos and that of g_{m6} is 288.7 μmhos, hence the approximate voltage gain at first stage is equal to 5.5 (≈15dB).

Due to the positive feedback gain is effectively squared (A_{V1}^2) or doubled in terms of dB.. The gain (28 dB) of the input stage obtained through simulation and presented in Figure 10 closely matches this predicted gain value.

The gain in the second stage of the comparator is computed by using the following expression

$$A_{V2} = \frac{g_{m8}}{g_{o8} + g_{o12}} \qquad (7)$$

In the above expression g_{m8} is the transconductance parameter of M_8 whose value is computed to be as 577.4µmhos approximately. The parameters g_{o8} and g_{o12} are the output transconductance's of transistors M_8 and M_{12} whose values are calculated to be as 10.9µmhos and 4.5µmhos respectively.

In computing the output conductance's, the Early voltages for the transistors are obtained by performing simulations on transistors M_8 and M_{12}. The value of Early voltage for the PFET, M_8, which has a length of 0.48 µm is 18 V and the Early Voltage of the NFET M_{12}, which has a length of 1.98µm is 45 V. Substituting the values of g_{m8}, g_{o8} and g_{o12} in equation (7), the second stage gain of the comparator is estimated to be as 37.5 (≈31.5dB). The overall voltage gain is the product of first and second stage gains which is equal to 1134 (≈61.1dB).

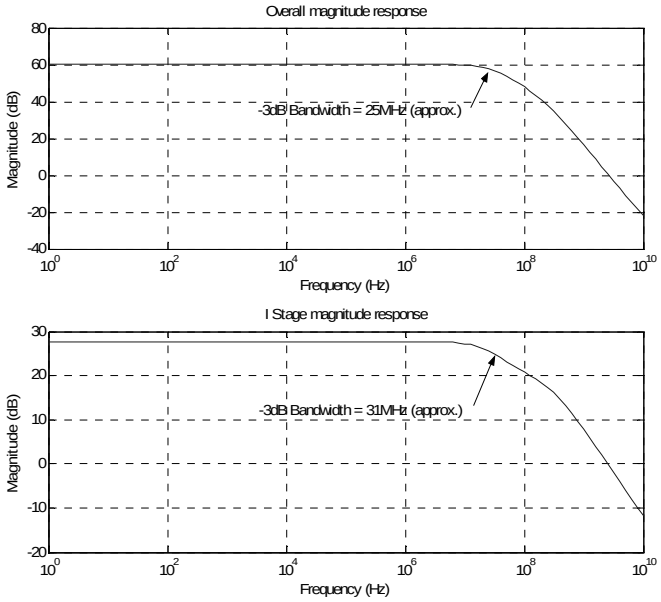

Figure 10. AC magnitude response of the comparator

The magnitude response shown in Figure 10 is indicating an overall gain of 60.3dB and is close to the predicted value. The comparator outputs shown in Figure 9 are buffered through two inverters whose PFETs are 0.96μm x 0.24μm and the NFETs are 0.36μm x 0.24μm.

The load at node '`I`' shown in Figure 9 of the comparator is estimated to be as 645fF. This is the load at the first stage of the comparator. The gain bandwidth product of the comparator is computed by using the expression given below

$$GBW = \frac{g_{m4}}{2\pi C_{LI}} \qquad (8)$$

where C_{LI} is the load at node '`I`'. The gain bandwidth product is approximately equal to 395MHz and when this value is divided by the overall gain, the bandwidth of the comparator is obtained. The estimated bandwidth of the comparator is approximately equal to 13MHz. The simulated bandwidth shown in Figure 10 at the first stage of is

approximately equal to 31MHz. Due to high bandwidth and high output voltage swing of the analog multipliers; the reduced bandwidth of the comparator has little effect on the overall clock generators operation.

3.3 SR Latch

The clock generator's '*Init!*' and '*Done!*' signals are latched by SR latches. The outputs of SR latches are applied to an OR gate (with active low inputs) whose output starts and stops the clock generator. The circuit for the SR latch is realized by two cross coupled NAND gates. The NAND gates are fully complementary logic structures. As illustrated in Figure 3, the 'S' and 'R' inputs of both the latches are active low signals. The inputs to the OR gate are also active low signals, hence inverting outputs of SR latches drive the inputs to the OR gate.

The 'R' input on both the latches is tied to the '*Done!*' input of the clock generator. The outputs of the latches are reset whenever the '*Done!*' signal is low, which indicates the "stop" of the clock. The active low 'S' inputs on the latches are connected to the '*Init!*' signal inputs of the clock generator. A low on anyone of the '*Init!*' signals sets the corresponding latch output which indicates the "start" of the clock.

3.5 Sample and Hold

The sample and hold circuit design is a simple transmission gate based switch and a sampling capacitor (100 fF). A schematic for the sample and hold appears in Figure 11.

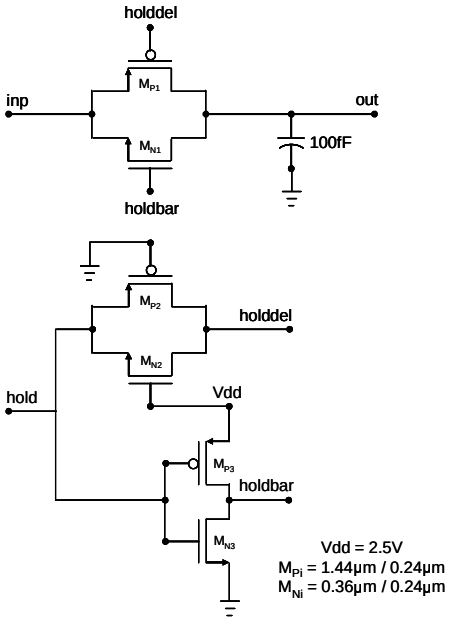

Figure 11. Sample and hold schematic

The sample and hold circuit shown above will be in sampling mode as long as the hold signal is low. In this state the input is freely passed to the output. The circuit goes to hold mode when the hold signal is high and starts holding the output from that instant.

The bandwidth of the sample and hold circuit has been simulated and is shown in Figure 12. The simulated bandwidth of the S/H is 130MHz. Due to the limited bandwidth of the sample and hold circuits, the overall bandwidth of the clock generator is limited. The shape factor's of the transistors in the transmission gate needs to be increased in order to improve the overall bandwidth of the clock generator.

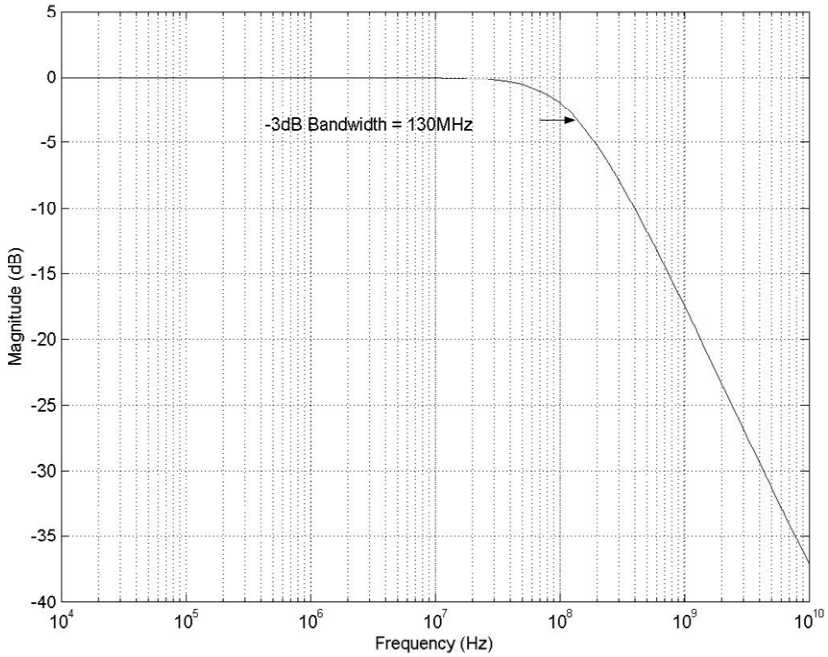

Figure 12. Frequency response of the sample and hold circuit

4.0 Results

Correct operation of the clock generator is illustrated in Figure 13. The sinewave input in the figure is one of the four quadrature inputs that is applied to the multiplier. The square wave output which acts as clock to the data processing subsystem, is started whenever the '*Init1!*' signal is pulsed low and is stopped when the '*Done!*' signal is pulsed low and is restarted with the next '*Init1!*' signal.

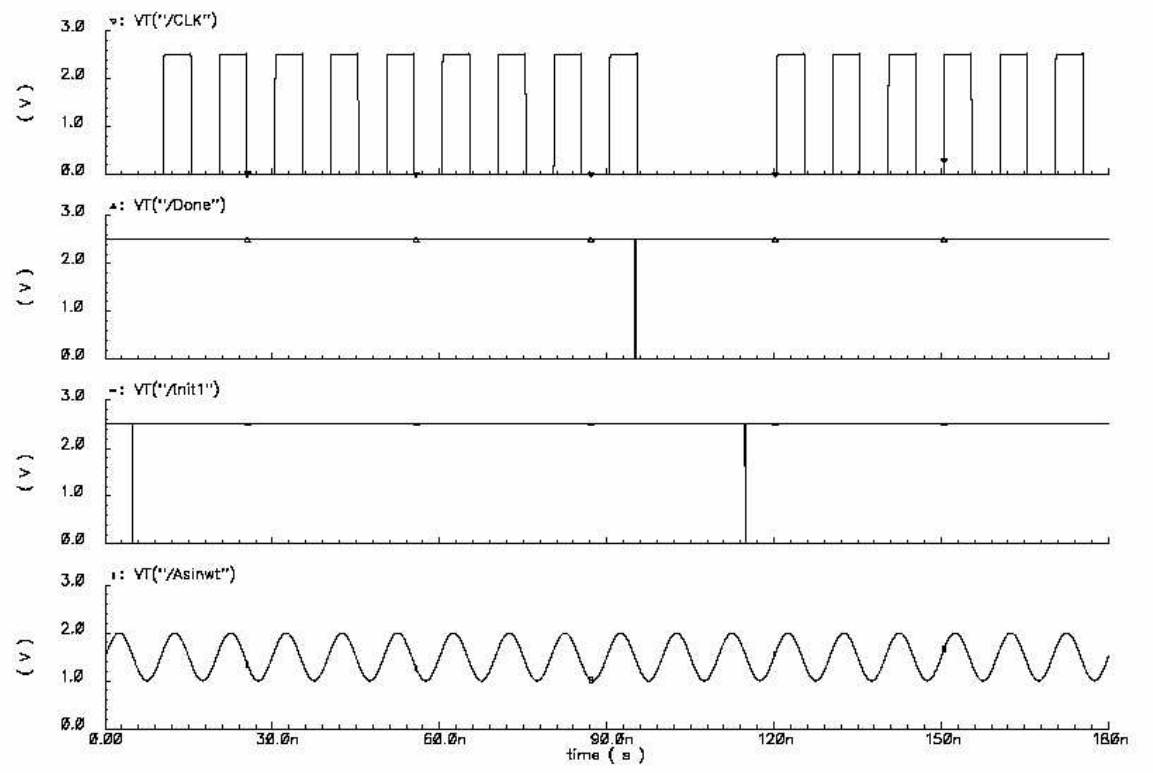

Figure 13. Functional verification of the clock generator

Figure 14 shows the delay that has been inserted from the rising edge of the '*Init!*' signal to the rising edge of the output clock. The graph is generated by distributing the '*Init!*' signal over one period of the input sinusoid whose frequency is 80MHz and the delay inserted is calculated from the falling edge of the '*Init!*' signal to the first rising edge of the clock.

The delay inserted is approximately half the period of the sinusoid and the peak-to-peak variation is 89 psec. This delay includes the delay inserted by SR latches, the OR gate, sample and hold circuits, multipliers, and the comparator.

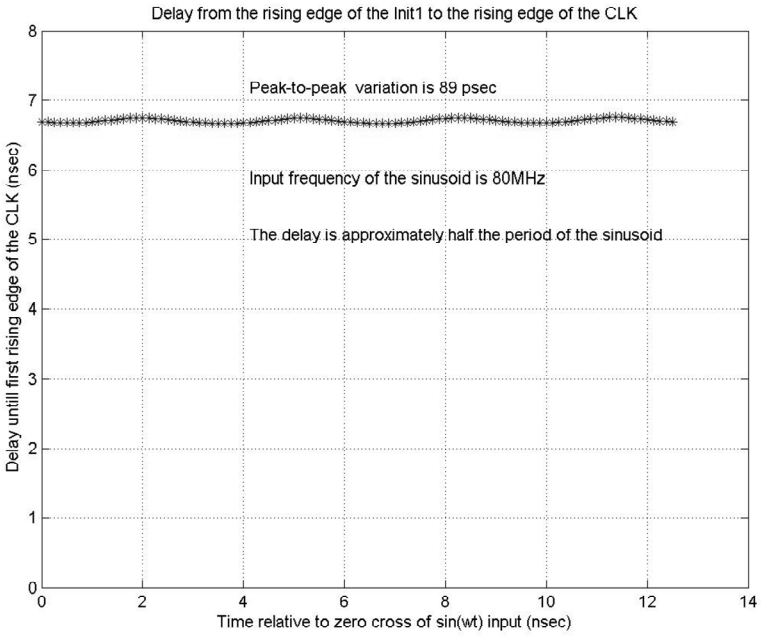

Figure 14. Delay measurement

The simulated frequency response of the clock generator (less the comparator) has been obtained and is illustrated in Figure 15. The -3dB bandwidth is approximately 280MHz.

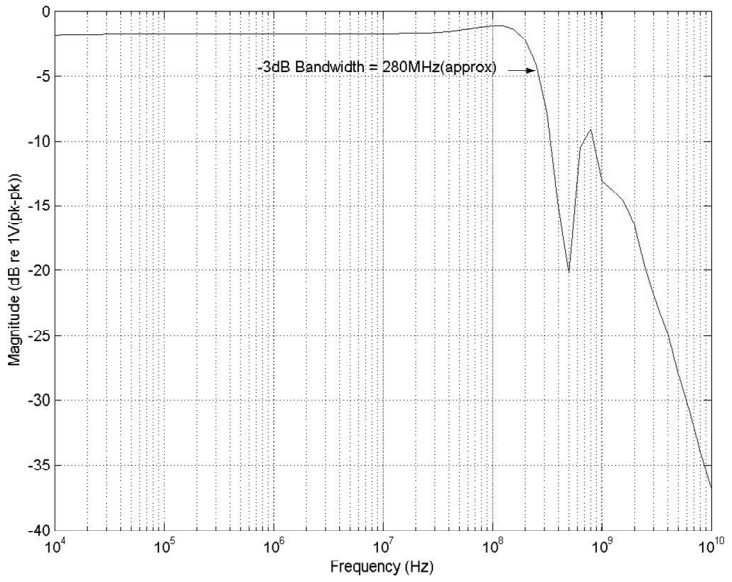

Figure 15. Frequency response of the clock generator (less comparator)

The improvement in the bandwidth of the clock generator can be obtained by improving the bandwidth of the sample and hold circuits. Figure 16 illustrates the increased bandwidth of the clock generator when the bandwidth of the sample and hold circuits has been increased to 600MHz.

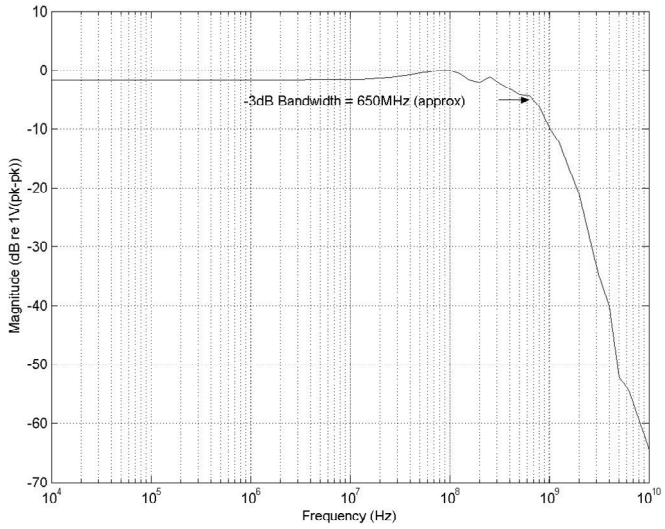

Figure 16. Improved frequency response of the clock generator (less comparator)

The improvement in the bandwidth of the sample and hold circuits is obtained by increasing the shape factor of the transmission gate (lowering the ON resistance of the switch) with 100fF load shown in Figure 11. The shape factor has been increased by a factor of 6.

The clock generator has a static power dissipation of 20mW. Approximately eighty percent of the power is dissipated by the multipliers. Each multiplier draws 3mA of current.. The comparator requires draws 1mA of current. Fifteen percent of the total power is dissipated by the comparator. A pie chart indicating the various contributions by the subcircuits is shown in Figure 17.

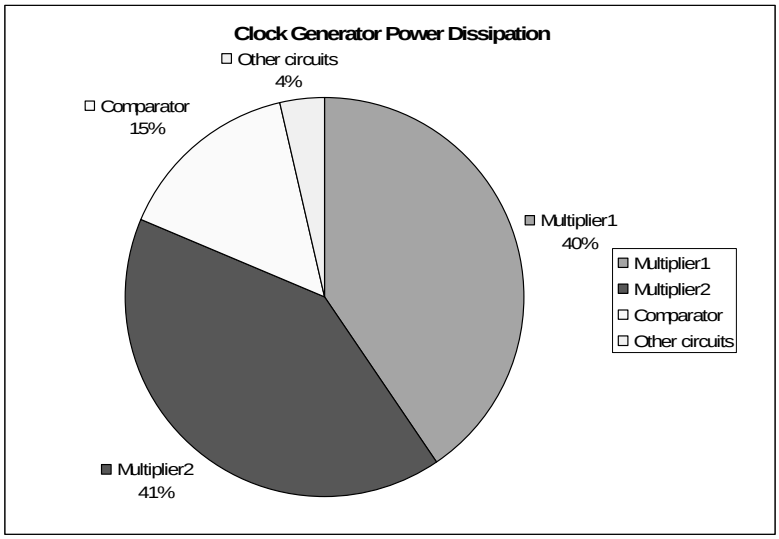

Figure 17. Pie chart indicating the power dissipation of the clock generator

5.0 Layout

A 28-pin test chip which consists of the clock generator, the analog multiplier, a quadrature VCO, and a 10GHz VCO has been submitted for fabrication thorough MOSIS under the TSMC 0.25 micron process. The dimensions of the chip are 1851μm x 1538μm with a total area of 2.847mm^2. The resistors are implemented by using a high resistance polysilicon layer.

The clock generator in the test chip has an area of 0.016mm^2. The output of the clock generator is made probable on the chip by connecting it to a 20μm x 20μm bonding pad and is also connected to a digital pad on the test chip. This allows us to obtain the characteristics of the clock generator both off-chip and on-chip.

Probe pads were also attached to four outputs of the QVCO and two outputs of the 10GHz VCO. This allows for the output frequency measurement of these circuits on the chip.

The outputs of the analog multiplier are brought out of the chip by connecting them to the analog reference pads. This allows us to characterize the analog multiplier at low frequencies. A sample resistor which is used in the analog multiplier is also made probable to test the resistance value on-chip.

A pie chart indicating the percentage area occupied by each component of the clock generator is presented in Figure 18.

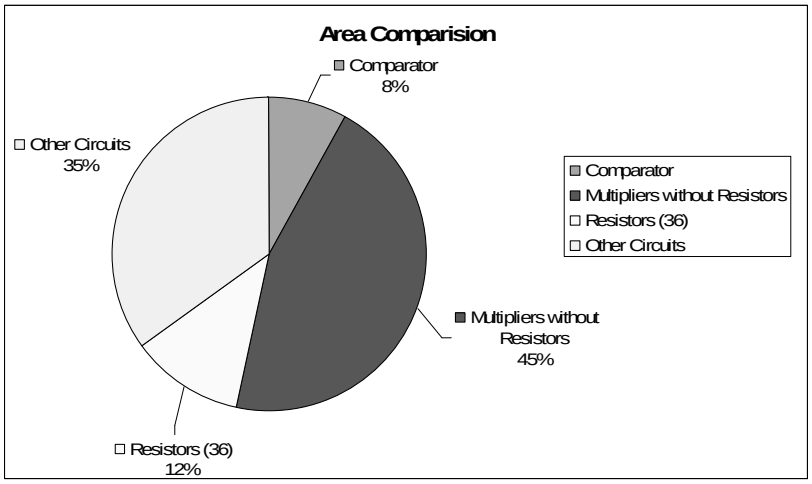

Figure 18. Pie chart indicating the area occupied by the sub circuits

6.0 Future Work

The bandwidth of the clock generator, delay inserted from '*Init!*' to the first rising edge of clock output and stopping the clock at the exact moment after the '*Done!*' pulse comes

along, are the important criteria that are to be considered for improving the overall performance of the clock generator. The bandwidth of the sample and hold circuits is to be improved which improves the bandwidth of the clock generator. This can be done by proper sizing of transistors in the sample and hold circuits. The total delay inserted from '*Init!*' to the rising edge of the clock can be improved only by reducing the delays inserted from latches to the comparator. This requires more analysis and simulations on the clock generator. The results obtained after testing the test chip that was submitted through MOSIS helps us to learn more and to take future decisions to improve the performance of the clock generator.

7.0 Acknowledgements

The author would like to thank Dr. George L. Engel for his invaluable support, patience and for his guidance throughout the length of this project without which this work could have not been achieved. The author would also like to thank Dr. Jerome R. Cox, Senior Professor, Department of Computer Science, Washington University, St. Louis on whose idea the entire project has been developed and implemented. His constant support throughout the project has been invaluable. Special thanks goes to David M. Zar, Department of Computer Science, Washington University, St. Louis for his support and suggestions in implementing the project and helping us in getting the test chip fabricated through MOSIS. The author would like to specially thank Muthu Kumar Sadasivam, for his valuable suggestions concerning OCEAN scripts and in implementing the layout.

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